In th Claims

Claims 1-51 (Cancel)

Claim 52 (New): An array of memory cells comprising:

a set of capacitor constructions, the set of capacitor constructions being defined to include a first subset of capacitor constructions and a second subset of capacitor constructions;

a first wordline over the set of capacitor constructions, the first wordline being in electrical connection with the first subset of capacitor constructions;

a second wordline over the first wordline and in electrical connection with the second subset of capacitor constructions; and

wherein the first wordline does not electrically connect with the second subset of capacitor constructions and the second wordline does not electrically connect with the first subset of capacitor constructions.

Claim 53 (New): The array of claim 52 wherein the second wordline is over the set of capacitor constructions.

Claim 54 (New): The array of claim 53 further comprising:

openings extending through the first wordline and proximate the second subset of capacitor constructions;

sidewall spacers within the openings and narrowing the openings; and

conductive material within the openings, the conductive material electrically connecting the second wordline to the second subset of capacitor constructions.

Claim 55 (New): The array of claim 54 wherein the conductive material comprises conductively-doped silicon.

Claim 56 (New): The array of claim 53 wherein the first and second wordlines comprise conductively-doped silicon.

Claim 57 (New): The array of claim 53 further comprising an insulative material layer over the second subset of capacitor constructions; the insulative material layer physically and electrically separating the second subset of capacitor constructions from the first wordline.

Claim 58 (New): The array of claim 57 wherein the insulative material layer comprises silicon nitride.

Claim 59 (New): The array of claim 53 further comprising:

a semiconductive material over the set of capacitor constructions;

source/drain regions within the semiconductive material, the source/drain regions being proximate at least some of the first and second wordlines;

openings extending through the first and second wordlines and to the source/drain regions; and

bitline interconnections within the openings and electrically connected through the source/drain regions to the set of capacitor constructions.

Claim 60 (New): An array of memory cells comprising:

a set of transistor gates, the set of transistor gates being defined to include a first subset of transistor gates and a second subset of transistor gates;

a first wordline over the set of transistor gates and electrically connected to the first subset of transistor gates;

a second wordline over the first wordline and electrically connected to the second subset of transistor gates; and

wherein the first wordline does not electrically connect with the second subset of transistor gates and the second wordline does not electrically connect with the first subset of transistor gates.

Claim 61 (New): The array of claim 60 wherein the second wordline is over the set of transistor gates.

Claim 62 (New): The array of claim 61 wherein the second wordline is directly over the first wordline.

Claim 63 (New): The array of claim 61 further comprising:

openings extending through the first wordline and to the second subset of transistor gates;

sidewall spacers within the openings and narrowing the openings; and

conductive material within the openings, the conductive material electrically connecting the second wordline to the second subset of transistor gates.

Claim 64 (New): The array of claim 63 wherein the conductive material comprises conductively-doped silicon.

Claim 65 (New): The array of claim 61 wherein the first and second wordlines comprise conductively-doped silicon.

Claim 66 (New): The array of claim 61 wherein the first wordline is physically against the first subset of transistor gates, and further comprises an insulative material layer over the second subset of transistor gates; the insulative material layer physically and electrically separating the second subset of transistor gates from the first wordline.

Claim 67 (New): The array of claim 66 wherein the insulative material layer comprises silicon nitride.

Claim 68 (New): The array of claim 61 further comprising:

a semiconductive material under the first and second subset of transistor gates and over capacitor constructions;

conductively doped source/drain regions within the semiconductive material, the source/drain regions being proximate at least some of the first and second subset of transistor gates;

openings extending through the first and second wordlines and to the source/drain regions; and

bitline interconnections within the openings and electrically connected through the first and second subset of transistor gates to the capacitor constructions.

Claim 69 (New): An array of memory cells comprising:

a set of transistor gates, the set of transistor gates defining a first subset of transistor gates and a second subset of transistor gates;

a first conductive line over the set of transistor gates and electrically connected to the first subset of transistor gates; and

a second conductive line between the first conductive line and the set of transistor gates, the second conductive line being electrically connected to the second subset of transistor gates.

Claim 70 (New): The array of claim 69 wherein the first conductive line is directly over the second conductive line.

Claim 71 (New): The array of claim 69 wherein the first and second conductive lines comprise conductively-doped silicon.

Claim 72 (New): The array of claim 69 further comprising:

a semiconductive material under the set of transistor gates and over capacitor constructions;

conductively doped source/drain regions within the semiconductive material, the source/drain regions being proximate at least some of the set of transistor gates;

openings extending through the first and second conductive lines and to the source/drain regions; and

bitline interconnections within the openings and electrically connected through the set of transistor gates to the capacitor constructions.